AN14284

Timing Parameter Tuning for FlexIO Emulated Interface

Rev. 1 — 12 April 2024 Application note

Document information

Information	Content
Keywords	AN14284, FlexIO, SPI
Abstract	This application note describes how to use additional timers to tune the setup time in SPI master in RT1170-EVK.

1 Introduction

FlexIO is an on-chip peripheral available on Kinetis, S32K, RT, and MCX microcontroller families. It is highly configurable and capable of emulating a wide range of communication protocols, such as UART, I^2C, SPI, I^2S, and LIN and others more like J1850, I3C, Manchester.[1]

The standalone peripheral module FlexIO is used as an additional peripheral module of the microcontroller and is not a replacement of any communication peripheral.

The key feature of FlexIO is its flexibility, which enables users to customize even timing parameters.

This application note describes how to use additional timers to tune the setup time in SPI master in RT1170-EVK.

2 Emulation of SPI master

2.1 Overview

To emulate SPI master in FlexIO, these resources are used:

- Two shifters: One is a transmitter and the other is a receiver.
- Two timers: One is used for the chip select generation, and the other is used for clock generation to control two shifters.
- Four pins: CS, SCK, MOSI, and MISO.

2.2 Receiving error at a high baud rate

The driver to emulate SPI master is typically included in the MCUXpresso SDK. Here is the result when `evkmimxrt1170_flexio_spi_edma_lpspi_transfer_master_cm7` is running at 20 MHz.

SPI master receives one-bit shifted data and error occurs somehow as shown below.

```
FLEXIO Master edma - LPSPI Slave edma example start.
This example use one flexio spi as master and one lpspi instance as slave on one board.
Master uses edma and slave uses edma way.
Please make sure you make the correct line connection. Basically, the connection is:
FLEXIO_SPI_master -- LPSPI_slave
       CLK        --    CLK
       PCS        --    PCS
       SOUT       --    SIN
       SIN        --    SOUT
This is LPSPI slave call back.

 Master receives:
       FF   FF   FE   FE   FD   FD   FC   FC   FB   FB   FA   FA   F9   F9   F8   F8
       F7   F7   F6   F6   F5   F5   F4   F4   F3   F3   F2   F2   F1   F1   F0   F0
 Slave transmits:
       FF   FE   FD   FC   FB   FA   F9   F8   F7   F6   F5   F4   F3   F2   F1   F0
       EF   EE   ED   EC   EB   EA   E9   E8   E7   E6   E5   E4   E3   E2   E1   E0
Error occurred in FLEXIO SPI master <-> LPSPI slave transfer!

End of example.
```

1 Using FlexIO to emulate Quad SPI master (document AN14175)

Using FlexIO to emulate communications and timing peripherals (document AN12174)

Figure 1 shows the signals measured by the logic analyzer.

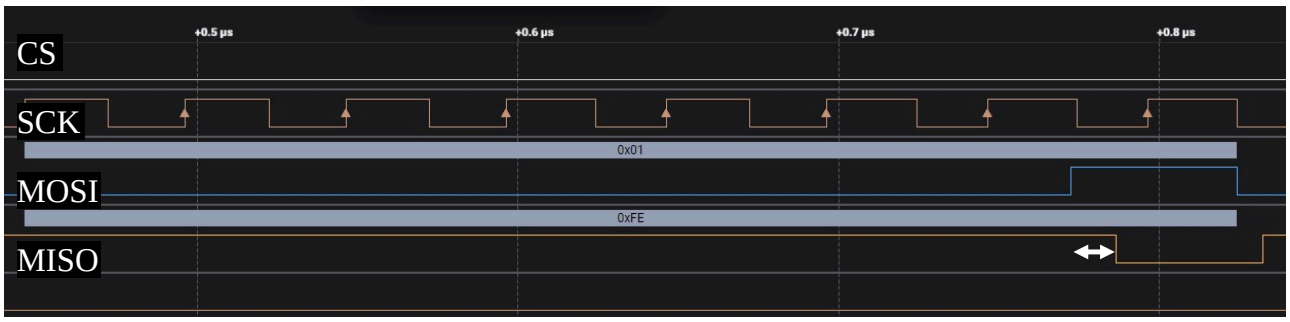

Figure 1. MISO is a little behind the SCK

MISO is a little bit behind the SCK because the slave device is driven by the master device, but MISO is sampled by the positive edge of SCK. That results in a one-bit shifted data.

This is what is called setup time. Latency depends on how fast the connected slave device is.

3 Setup time tuning by delayed clock

3.1 What is a delayed clock

In naive implementation, the receiver is shifted by the positive edge of SCK, which results in a one-bit shift when MOSI is a little behind the SCK. By using the internal delayed clock for the receiver, the master receives correct data even if MOSI is behind the SCK.

3.2 Configuring the shifters and timers

Additional four timers are needed to realize the delayed clock. While the transmit shifter is controlled by SCK as usual, the receive shifter is controlled by Delayed SCK. The output of each timer must follow the timing chart, as shown in Figure 2.

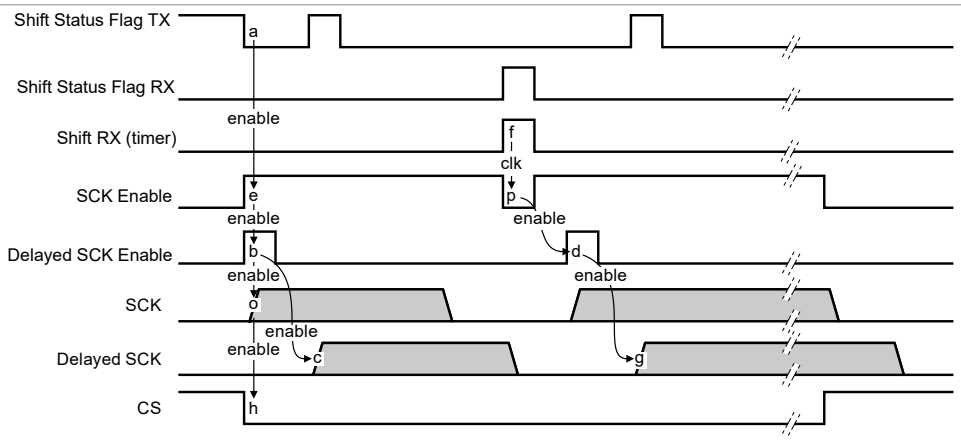

Figure 2. Timing chart

- Shifter RX is added to convert Shifter Status Flag (SSF) into timer output. It is used for SCK Enable.
- SCK is enabled when SCK Enabled is asserted. SCK Enable is asserted when SSF TX is low and SSF RX falls.

- Delayed SCK is enabled when Delayed SCK Enable is asserted. Delayed SCK Enable counts how much Delayed SCK should be delayed. One unit is one FlexIO cycle. In the demo, Delayed SCK is configured to count two cycles, but it is customizable.

Concretely, timers are configured as follows.

Table 1. Timer configuration

Timer	Name	Trigger select	Pin select	Enable condition	Disable condition	Decrement source
0	Shifter RX	SSF RX	Output (ShifterRxPin)	Trigger rising	Timer compare	Trigger
1	SCK Enable	SSF TX	Input (ShifterRxPin)	Trigger low	Timer compare	Pin
2	Delayed SCK Enable	SCK Enable	Not used	Trigger rising	Timer compare	FlexIO clock
3	SCK	SCK Enable	Output (SCKPin)	Trigger rising	Timer compare	FlexIO clock
4	Delayed SCK	Delayed SCK Enable	Output (DelayedSCKPin)	Trigger rising	Timer compare	FlexIO clock
5	CS	SCK Enable	Output (CSnPin)	Trigger rising	Timer compare	trigger

3.3 Running the demo

To make the example work, connections are as shown in Table 2.

Table 2. Pin connection

Signal	Slave	Master
MOSI	J10-10	J26-6
MISO	J10-8	J26-4
SCK	J10-12	J26-2
Delayed SCK (Test point)	—	J26-10
CS	J10-6	J26-8

1. Remove 0Ω resistor to R200,R406,R408, and R404.
2. Connect a mini USB cable between the PC host and the OpenSDA USB port on the board.
3. Open a serial terminal on the computer for OpenSDA serial device with these settings:
   - 115200 baud rate
   - 8 data bits
   - No parity
   - One stop bit
   - No flow control
4. Download the program to the target board.
5. Either press the reset button on your board or launch the debugger in your IDE to begin running the demo.

You can see the following message in the terminal if the example runs successfully.

```
FLEXIO Master edma - LPSPI Slave edma example start.
This example use one flexio spi as master and one lpspi instance as slave on one board.
Master uses edma and slave uses edma way.
Please make sure you make the correct line connection. Basically, the connection is:
FLEXIO_SPI_master -- LPSPI_slave
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This is LPSPI slave call back.

 Master receives:
       FF   FE   FD   FC   FB   FA   F9   F8   F7   F6   F5   F4   F3   F2   F1   F0
       EF   EE   ED   EC   EB   EA   E9   E8   E7   E6   E5   E4   E3   E2   E1   E0
 Slave transmits:
       FF   FE   FD   FC   FB   FA   F9   F8   F7   F6   F5   F4   F3   F2   F1   F0
       EF   EE   ED   EC   EB   EA   E9   E8   E7   E6   E5   E4   E3   E2   E1   E0
FLEXIO SPI master <-> LPSPI slave transfer all data matched!

End of example.
```

Figure 3 shows that Delayed SCK is a two-FlexIO cycle delayed as configured.

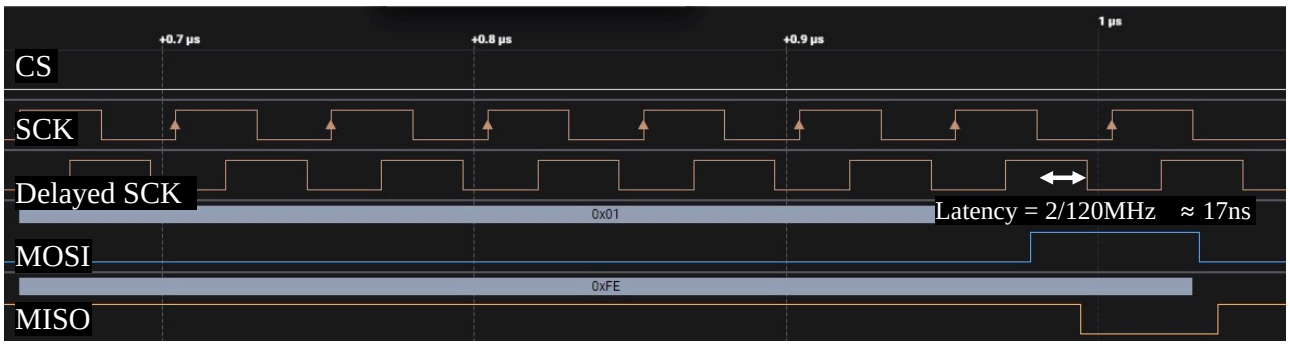

Figure 3. Delayed SCK is two-FlexIO cycle delayed

4 Conclusion

By using additional timers, even timing parameters can be customized in the FlexIO emulated interface.

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6 Revision history

Table 3 summarizes the revisions to this document.

Table 3. Revision history

Document ID	Release date	Description
AN14284 v.1	12 April 2024	Initial public release

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